high-concentration P-type impurity diffusion region located adjacently under the buried channel region that includes an aluminum or boron diffusion region having a maximum impurity concentration of 1 x 10^{17} cm^{-3} to 1 x 10^{19} cm^{-3}.

REMARKS

Favorable reconsideration, in light of the present amendments and following discussion, is respectfully requested.

Claims 2-16 and 18-42 are presently pending; Claims 1 and 17 have been canceled; and Claims 2 and 8-16 have been amended by the present amendment. No new claims have been added herewith. Applicants respectfully submit that no new matter has been added by the present amendment.

In the outstanding Office Action, Claims 1-11, 17-21, 39, and 40 were rejected under 35 U.S.C. § 103(a) as unpatentable over Pfiester (U.S. Pat. No. 4,714,519) in view of Ohno et al. (U.S. Pat. No. 5,736,753, hereafter Ohno); Claims 1, 2, 7, 12, 22, and 41 were rejected under 35 U.S.C. § 103(a) as unpatentable over Christie et al. (U.S. Pat. No. 4,017,888, hereafter Christie) in view of Ohno; Claims 13-16, 23, and 42 were rejected under 35 U.S.C. § 103(a) as unpatentable over Pfiester and Ohno as applied to Claim 10 above, and further in view of Christie; Claims 24-28, 30-34, and 38 were rejected under 35 U.S.C. § 103(a) as unpatentable over Pfiester and Ohno as applied to Claim 2 above, and further in view of Bulucea et al. (U.S. Pat. No. 5,952,701, hereafter Bulucea); and Claims 29, 32, and 35-37 were rejected under 35 U.S.C. § 103(a) as unpatentable over Christie and Ohno as applied to Claim 12 above, and further in view of Bulucea.

Applicants thank Examiner Nguyen and Supervisory Examiner Jackson for the interview granted Applicants' representatives on August 20, 2002. During the interview,

proposed amendments, as filed herewith, to Claim 2 were discussed with relation to the references of record. Applicants' representatives pointed out that none of the references of record disclose or suggest the particular ratios claimed by independent Claim 2. It was agreed that the Examiner would further consider Applicants' comments in light of the interview discussion and discussed amendments.

In response to the rejection of Claims 1-11, 17-21, 39, and 40 under 35 U.S.C. § 103(a) as unpatentable over Pfiester in view of Ohno, that rejection is traversed by the present amendment.

Claims 1 and 17 have been canceled herewith. Claims 3-11, 18-21, 39, and 40 all depend from independent Claim 2. Claim 2 recites: "a SiC semiconductor device ... wherein a ratio (L_{bc}/X_j) is not less than 0.2 and not more than 1.0, where the L_{bc} is a depth of the buried channel region adjacent to a boundary formed by the N-type impurity region and the P-type silicon carbide region and the X_j is a depth of the source and drain regions." The Applicants' claimed configuration has high hot-carrier endurance, high punch-through endurance, and high channel mobility.[2]

At the outset, it is noted that none of the references of record discloses or suggests any type of ratio between layers equivalent to the claimed ratio (L_{bc}/X_j). Specifically, none of the references discloses or suggests that a ratio similar to the claimed ratio may be beneficial in any way.

Pfiester relates to a method for fabricating MOS transistors having gates with different work functions. As noted above, Pfiester fails to disclose or suggest any ratio similar to the ratio recited in pending Claim 2. Further, as noted in the Office Action, Pfiester fails to

[2]Specification, page 2, lines 18-21.

disclose or suggest a silicon carbide region.[3]

The Office Action attempts to remedy this admitted deficiency by relying on Ohno. Ohno relates to a semiconductor device for improved power conversion having a hexagonal system single crystal silicon carbide. However, Ohno fails to disclose or suggest a ratio as claimed in Claim 2. Specifically, Ohno fails to disclose or suggest "a SiC semiconductor device ... wherein a ratio (L_{bc}/X_j) is not less than 0.2 and not more than 1.0, where the L_{bc} is a depth of the buried channel region adjacent to a boundary formed by the N-type impurity region and the P-type silicon carbide region and the X_j is a depth of the source and drain regions." Accordingly, Applicants respectfully submit that Ohno fails to remedy the defects above-noted with respect to Pfiester.

Consequently, Applicants respectfully submit that pending independent Claim 2 patentably distinguishes over Pfeister and Ohno, either alone or in combination. Likewise, pending dependent Claims 3-11, 18-21, 39, and 40 are considered to patentably distinguish over the cited references, either alone or in combination, for at least the reasons above-noted with respect to independent Claim 2, from which these claims depend. Applicants therefore respectfully request that this rejection be withdrawn.

With regard to the rejection of Claims 1, 2, 7, 12, 22, and 41 under 35 U.S.C. § 103(a) as unpatentable over Christie in view of Ohno, that rejection is traversed by the present response. Claim 1 has been canceled herewith. Claims 7, 12, 22, and 41 depend from Claim 2. As noted above, Claim 2 recites: "a SiC semiconductor device ... wherein a ratio (L_{bc}/X_j) is not less than 0.2 and not more than 1.0, where the L_{bc} is a depth of the buried channel region adjacent to a boundary formed by the N-type impurity region and the P-type silicon

[3]Office Action, page 2.

carbide region and the X_j is a depth of the source and drain regions."

Christie relates to a non-volatile metal nitride oxide semiconductor device. As noted in the Office Action, Christie fails to disclose or suggest any type of silicon carbide region.[4] As Christie fails to disclose or suggest any type of silicon carbide region, Christie necessarily fails to disclose or suggest: "a SiC semiconductor device ... wherein a ratio (L_{bc}/X_j) is not less than 0.2 and not more than 1.0, where the L_{bc} is a depth of the buried channel region adjacent to a boundary formed by the N-type impurity region and the P-type silicon carbide region and the X_j is a depth of the source and drain regions."

Again, the Office Action attempts to use Ohno to remedy the admitted defects of Christie. However, as noted above, Ohno fails to disclose or suggest "a SiC semiconductor device ... wherein a ratio (L_{bc}/X_j) is not less than 0.2 and not more than 1.0, where the L_{bc} is a depth of the buried channel region adjacent to a boundary formed by the N-type impurity region and the P-type silicon carbide region and the X_j is a depth of the source and drain regions."

Accordingly, Applicants respectfully submit that pending independent Claim 2 patentably distinguishes over Christie and Ohno, either alone or in combination. Likewise, pending dependent Claims 7, 12, 22, and 41 patentably distinguish over Christie and Ohno, either alone or in combination, for at least the reasons above-noted with respect to Claim 2, from which these claims depend. Applicants therefore respectfully request that this rejection be withdrawn.

In response to the rejection of Claims 13-16, 23, and 42 under 35 U.S.C. § 103(a) as unpatentable over Pfeister and Ohno as applied to Claim 10, and further in view of Christie,

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[4]Office Action, page 3.

that rejection is traversed by the present response. Claims 13-16, 23, and 42 all depend from Claim 2.

As noted above, Pfeister fails to disclose or suggest the limitations recited in pending Claim 2. As further noted above, Ohno fails to remedy the defects above-noted and admitted in the Office Action with respect to Pfeister. As further noted above, Christie fails to remedy the defects above-noted with respect to Pfeister and Ohno. Specifically, none of these references, either alone or in combination, disclose or suggest: "a SiC semiconductor device ... wherein a ratio (L_{bc}/X_j) is not less than 0.2 and not more than 1.0, where the L_{bc} is a depth of the buried channel region adjacent to a boundary formed by the N-type impurity region and the P-type silicon carbide region and the X_j is a depth of the source and drain regions."

Accordingly, as Pfeister, Ohno, and Christie all fail to disclose or suggest the features recited in pending independent Claim 2, from which Claims 13, 16, 23, and 42 depend, Applicants respectfully request that this rejection be withdrawn.

In response to the rejection of Claims 24-28, 30-34, and 38 under 35 U.S.C. § 103(a) as unpatentable over Pfeister and Ohno as applied to Claim 2, and further in view of Bulucea, Applicants respectfully submit that Bulucea fails to remedy the defects above-noted with respect to Pfeister and Ohno.

Bulucea relates to the design and fabrication of semiconductor structure having complimentary channel-junction insulated-gate field-effect transistors. However, Bulucea also fails to disclose or suggest "a SiC semiconductor device ... wherein a ratio (L_{bc}/X_j) is not less than 0.2 and not more than 1.0, where the L_{bc} is a depth of the buried channel region adjacent to a boundary formed by the N-type impurity region and the P-type silicon carbide region and the X_j is a depth of the source and drain regions."

Accordingly, as neither Pfeister, Ohno, nor Bulucea discloses or suggests the

limitations recited in pending independent Claim 2, Applicants respectfully submit that pending independent Claim 2 patentably distinguishes over these three references, either alone or in combination. Likewise, pending dependent Claims 24-28, 30-34, and 38 are considered to patentably distinguish over the cited references, either alone or in combination, for at least the reasons above-noted with respect to Claim 2, from which these claims depend.

In response to the rejection of Claims 29, 32, and 35-37 under 35 U.S.C. § 103(a) as unpatentable over Christie and Ohno as applied to Claim 12, and further in view of Bulucea, that rejection is traversed by the present response. Claim 2, from which Claims 29, 32, and 35-37 depend, recites: "a SiC semiconductor device ... wherein a ratio (L_{bc}/X_j) is not less than 0.2 and not more than 1.0, where the L_{bc} is a depth of the buried channel region adjacent to a boundary formed by the N-type impurity region and the P-type silicon carbide region and the X_j is a depth of the source and drain regions."

As noted above, Christie, Ohno, and Bulucea all fail to disclose or suggest the features recited in pending independent Claim 2. Accordingly, pending dependent Claims 29, 32, 35, and 35-37 are considered to patentably distinguish over Christie, Ohno, and Bulucea, either alone or in combination, for at least the reasons above-noted with respect to independent Claim 2. Applicants therefore respectfully request that this rejection be withdrawn.

Consequently, in view of the foregoing discussion and present amendments, Applicants respectfully submit that the pending application is in condition for immediate allowance. An early and favorable action is therefore respectfully requested.

Respectfully submitted,

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IN THE CLAIMS

1. (Canceled)

2. (Amended) [A device according to claim 1] A SiC semiconductor device comprising:

a semiconductor substrate having a P-type silicon carbide region, a gate insulation layer formed on the silicon carbide region;

an effective P-type gate electrode formed on the gate insulation layer, an N-type impurity region having an impurity concentration sufficient to form a buried channel region in a semiconductor layer on a lower surface of the gate insulation layer, a diffusion region formed in the semiconductor substrate; and

source and drain regions comprised of N-type impurity regions formed adjacent to the gate insulation layer and gate electrode,

wherein a ratio (L_{bc}/X_j) is not less than 0.2 and not more than 1.0, where the L_{bc} is a depth [from an interface between the gate insulation layer and the silicon carbide] of the buried channel region adjacent to a boundary formed by the N-type impurity region and the P-type silicon carbide region [region to the buried channel region], and the X_j is a depth [from the interface between the gate insulation layer and the silicon carbide region to a junction] of the source and drain regions.

8. (Amended) A device according to claim 2, wherein [between the buried channel region and the source and drain regions there is a] the diffusion region [having] has an impurity concentration that is not lower than a maximum impurity concentration of the impurity region used to form the buried channel region and not higher than an impurity concentration of the source or drain regions.

9. (Amended) A device according to claim 7, wherein [between the buried channel region and the source and drain regions there is a] the diffusion region [having] has an impurity concentration that is not lower than a maximum impurity concentration of the impurity region used to form the buried channel region and not higher than an impurity concentration of the source or drain regions.

10. (Amended) A device according to claim 8, wherein [between the buried channel region and the source and drain regions there is a] the diffusion [layer] region comprises [of] nitrogen, phosphorus, or arsenic at a maximum concentration that is from 5×10^{16} cm^{-3} to 1×10^{19} cm^{-3}.

11. (Amended) A device according to claim 9, wherein [between the buried channel region and the source and drain regions there is a] the diffusion [layer] region comprises [of] nitrogen, phosphorus, or arsenic at a maximum concentration that is from 5×10^{16} cm^{-3} to 1×10^{19} cm^{-3}.

12. (Amended) A device according to claim 7, wherein [there] the diffusion region is a P-type impurity diffusion region having an impurity concentration that is higher than an

impurity concentration of the semiconductor substrate, said P-type impurity diffusion region being located adjacently under the buried channel region.

13. (Amended) A device according to claim 10, wherein [there] the diffusion region is a P-type impurity diffusion region having an impurity concentration that is higher than an impurity concentration of the semiconductor substrate, said P-type impurity diffusion region being located adjacently under the buried channel region.

14. (Amended) A device according to claim 11, wherein [there] the diffusion region is a P-type impurity diffusion region having an impurity concentration that is higher than an impurity concentration of the semiconductor substrate, said P-type impurity diffusion region being located adjacently under the buried channel formation region.

15. (Amended) A device according to claim 13, wherein [there] the diffusion region is a high-concentration P-type impurity diffusion region located adjacently under the buried channel region that includes an aluminum or boron diffusion [layer] region having a maximum impurity concentration of 1×10^{17} cm^{-3} to 1×10^{19} cm^{-3}.

16. (Amended) A device according to claim 14, wherein [there] the diffusion region is a high-concentration P-type impurity diffusion region located adjacently under the buried channel region that includes an aluminum or boron diffusion [layer] region having a maximum impurity concentration of 1×10^{17} cm^{-3} to 1×10^{19} cm^{-3}.

17. (Canceled)